AMENDMENTS TO THE CLAIMS:

Please cancel claims 1-11 and 41, amend claim 37, and add new claims 42-47, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claims 1-11 (currently cancelled)

Claims 12-36 (previously cancelled)

Claim 37 (currently amended): A method for manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor substrate;

forming, on said semiconductor substrate, a first photoresist pattern layer using a first photomask having active area patterns corresponding to active areas and dummy area patterns corresponding to dummy areas; ~~on a semiconductor substrate;~~

forming a trench in said semiconductor substrate, which trench partitions pattern areas corresponding to said dummy area patterns from pattern areas corresponding to said active area patterns, by an etching process using said first photoresist pattern layer as an etching mask;

removing said first photoresist pattern layer;

burying insulating layers in said trenches after said first photoresist pattern layer is removed;

forming a conductive layer ~~over~~ on ~~said~~ semiconductor substrate;

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forming a second photoresist pattern layer on said conductive layer using a second photomask having gate patterns corresponding to said active areas and dummy gate patterns corresponding to said dummy areas; and

patterning said conductive layer by an etching process using said second photoresist pattern layer, each of said dummy gate patterns ~~being a reduction~~ having a reduced area of a ~~corresponding~~ respective one of said dummy area patterns.

Claim 38 (previously presented): The method as claimed in claim 37, wherein the shape of at least one said dummy area patterns and/or dummy gate patterns is a circle.

Claim 39 (previously presented): The method as claimed in claim 37, wherein a plurality of said dummy area patterns and/or dummy gate patterns are arranged in at least two rows and/or two columns.

Claim 40 (previously presented): The method as claimed in claim 39, wherein at least one said row is shifted from another said row and/or at least one column is shifted from another said column.

Claim 41 (currently cancelled)

Claim 42 (new): A method of manufacturing a semiconductor device, comprising:

performing a selective etching on a semiconductor substrate having first and second active areas and an isolation area intervening between said first and second active areas, thereby forming a grid-shaped trench in said isolation area of said semiconductor substrate to define a plurality of dummy regions each surrounded by said grid-shaped trench;

forming an insulating layer in said grid-shaped trench;

forming a conductive layer on said semiconductor substrate; and

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selectively removing said conductor layer to form a transistor gate over each of said first and second active areas and a dummy gate over each of said dummy regions, said dummy gate having a reduced shape area as compared to a shape area of a corresponding one of said dummy regions.

Claim 43 (new): The method as set forth in claim 42, wherein said insulating layer is formed by chemical mechanical polishing process.

Claim 44 (new): The method as set forth in claim 42, wherein said transistor gate and said dummy gate are formed by use of such a mask pattern that is derived by combining a transistor gate pattern and a dummy gate pattern which is obtained by reducing a mask pattern for forming said grid-shaped trench.

Claim 45 (new): A method of manufacturing a semiconductor device, comprising:

defining in a semiconductor substrate first and second element formation regions and an element isolation region isolating said first and second element formation regions from each other;

forming first and second gate electrodes over said first and second element formation regions, respectively; and

forming two or more dummy gates over said element isolation region between said first and second gate electrodes.

Claim 46 (new): The method as claimed in claim 45, wherein said element isolation region includes a grid-shaped trench, and each of said dummy gates having a shape that is relative to a portion of said element isolation region surrounded by said grid-shaped trench.

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Claim 47 (new): The method as claimed in claim 46, wherein each of said dummy gates has a shape that is reduced as compared to said portion of said element isolation region.

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AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes changes to FIG. 3C. This sheet, which includes FIGS. 3A-3C and replaces the original sheet including FIGS. 3A-3C. A marked copy of amended FIG. 3C is also enclosed.

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